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Washington, DC 20231

OFGS File No. : P/3156-3
Inventor : Takuro YAMAMOTO
Title : VIDEO DATA TRANSFER SYSTEM
Assignee : NEC Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

13 Pages of Specification including Abstract and Claims
3 Numbered Claims Calculated as 3 Claims for Fee Purposes
3 Sheets of Drawing Containing Figures 1 to 3.
X Declaration and Power of Attorney
X Priority is Claimed under 35 U.S.C. §119:
Convention Date April 30, 1997 for Japan Appln. S.N. 9-112117
X Certified Priority Application
X PTO-1449 with 4 references
X Assignment
X Return-Addressed Post Card

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Date of Signature

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VIDEO DATA TRANSFER SYSTEM

FIELD OF THE INVENTION

The present invention relates to a video data transfer system, and more particularly to a video data transfer system used in a graphic accelerator having a video input function.

BACKGROUND OF THE INVENTION

FIG. 3 is a block diagram showing an example of a conventional video data transfer system. As shown in the figure, video data decoded by a video decoder 11 is sent via a video port 12 to a graphic accelerator 30 having the video input function. Upon receiving video data, the graphic accelerator 30, which comprises a video processor 21, display control circuit 22, and a FIFO memory 24, causes the video processor 21 to perform predetermined signal processing for the received video data and outputs the processed video data to a frame buffer 14 via a frame buffer data bus 13 for storage in an internal off-screen memory 15.

Video data stored in the off-screen memory 15 is usually sent to the display control circuit 22 in the graphic accelerator 30 via the frame buffer data bus 13, converted to signals suitable for display, and then sent to a display 16. The frame buffer data bus 13, the frame buffer 14, and the off-screen memory 15 constitute a real time output path 25.

At the same time, video data sent from the off-screen

memory 15 via the frame buffer data bus 13 is stored temporarily in the FIFO memory 24 which is in the graphic accelerator 30 and which constitutes a path 27 via which video data is output at video capture time. The video data is then output to a system bus 17 of a computer or some other unit and sent to a system memory 18.

However, there are certain problems encountered in the course of the investigations towards the present invention. There is a problem with the conventional system described above that, because the frame buffer data bus 13 is occupied by video data to be displayed on the display 16, the frame buffer data bus 13 becomes a bottleneck of data capturing, thus reducing the capturing rate.

Conversely, while video capturing is executed, the frame buffer data bus 13 of the conventional video data transfer system described above is occupied by video data transferred to the system memory 18. This prevents video data in the off-screen memory 15 from being updated and decreases the amount of updated data to be sent to the display 16 during data capturing, thus reducing the video display rate.

SUMMARY OF THE INVENTION

The present invention seeks to solve the problems associated with the prior art described above. It is an object of the present invention is to provide a video data transfer system which increases the capturing rate of video data to be sent to the

system memory.

It is another object of the present invention to provide a video data transfer system which does not affect the display of data on a display even when video data is being captured.

Further objects of the present invention will become apparent in the entire disclosure.

To achieve the above object, an embodiment according to the present invention comprises a real time output path through which video data processed by a video processor is transferred to a display via a frame buffer and a capturing-only path which is independent of the real time output path and through which video data is sent to a system memory via a system bus.

According to the present invention, video data output from the video processor may be sent to the system bus through a capturing-only path, not via the frame buffer.

In addition, the real time output path through which video data is transferred to the display in real time and the capturing-only path through which video data is sent to the system memory are configured independently. This configuration prevents the display of video data on the display unit from being affected even when video data is being captured.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a first embodiment of the present invention.

FIG. 2 is a flowchart explaining an operation of the

embodiment of FIG. 1.

FIG. 3 is a block diagram of an example of a conventional system.

DETAILED DESCRIPTION

An embodiment of the present invention is described with reference to the attached drawings. FIG. 1 is a block diagram of the embodiment of the video data transfer system according to the present invention. As shown in FIG. 1, a video decoder 11 is connected via a video port 12 to a graphic accelerator 20 which has the video input function. This graphic accelerator 20 is connected to a frame buffer 14 via a frame buffer data bus 13, to a system memory 18 via a system bus 17, and to a display 16. The graphic accelerator 20 has a video processor 21, a display control circuit 22 , a gate 23, and a FIFO memory 24.

This embodiment comprises the video processor 21 which processes (e.g., reduces the size of) video data received from the video decoder 11, a real time output path 25 which transfers video data from the video processor 21 to the display 16 via the frame buffer 14, and a capturing-only path 26 which transfers video data from the video processor 21 to the system memory 18.

Of these components, the real time output path 25 comprises the frame buffer data bus 13 via which video data from the video processor 21 is sent to the frame buffer 14, the frame buffer 14 in which all image data including video data is stored, an off-screen memory 15 which is in the frame buffer 14 and in

which video data is stored, and the display control circuit 22 which enlarges or interpolates video data to control the output timing for display.

On the other hand, the capturing-only path 26 comprises the gate 23 which controls capturing and the FIFO (first-in, first-out) memory 24 in which video data is stored.

The operation of this embodiment is described with reference to the flowchart shown in FIG. 2. First, video data processed by the video decoder 11 (step 101) is input to the video processor 21 which performs such processing as size reduction (step 102). Then, control is passed to one of two paths: real time output path 25 and capturing-only path 26.

Video data sent to the real time output path 25 is stored in the off-screen memory 15 in the frame buffer 14 (step 103), read from the off-screen memory 15 (step 104), sent to the display control circuit 22 for enlargement or video-to-graphic conversion (step 105), and sent to the display 16 for real time display (step 106).

On the other hand, the system checks video data sent to the capturing-only path 26 if the video data is to be captured (step 107). If the video data is not to be captured, the system closes the gate 23 to prevent the video data from being sent (step 113). If the video data is to be captured, the system opens the gate 23 to allow the video data to be sent (step 108) and stores the video data in the FIFO memory 24 (step 109).

Then, the system checks the video data if it may be transferred to the system bus 17 (step 110). If the video data may be transferred, it is transferred to the system bus 17 and stored in the system memory 18 (step 111). If, in step 110, the system determines that the video data may not be transferred to the system bus 17 for some reason, the system checks the vertical synchronization signal data to see if the video data is the last part of a field (step 112). If the video data is not the last part of a filed, the system transfers the next data to the FIFO memory 24 (steps 108 and 109); if the video data is the last part of a field, the system closes the gate 23 to stop data transfer and suspends frame capturing (step 113).

As described above, video data from the video processor 21 is sent, not via the frame buffer 14 but via the capturing-only path 26, directly to the system bus 17. This means that video data may be captured into the system memory 18 regardless of the status of the real time output path 25.

On the other hand, video data is sent to the display 16 via the real time output path 25 provided independently of the capturing-only path 26. This means that video data may be sent to the display 16 at a constant rate regardless of whether or not data is being captured.

Embodiment

The configuration of the embodiment according to the present invention is detailed with reference to FIG. 1. The

graphic accelerator 20 with the video input function is implemented as a large scale integrated circuit (LSI). It comprises the video processor 21 which reduces the size of video data according to the YUV 16 bits, the real time output path 25 which is a 64-bit internal bus through which video data from the video processor 21 is sent to the display control circuit 22 via the frame buffer 14, and the capturing-only path 26 which is a 32-bit internal bus through which video data from the video processor 21 is sent to the FIFO memory 24 via the gate 23.

The real time output path 25 comprises the 64-bit frame buffer data bus 13, the 2M-byte to 4M-byte frame buffer 14 in which image data including video data is stored, the variable-length off-screen memory 15 which is in the frame buffer 14 and in which video data is stored, and the display control circuit 22 which switches data from video data to graphic image data and vice versa, enlarges video data according to a display size, performs interpolation, and converts analog RGB signals from digital to analog and vice versa.

On the other hand, the capturing-only path 26 comprises the gate 23 which enables/disables the FIFO memory 24 and the 32-bit-by-640-stage (YUV 16 bits, 2 lines of video data) FIFO memory 24.

The operation of the embodiment according to the present invention is described with reference to FIGS. 1 and 2. Upon receiving NTSC analog video signals, the video decoder 11

converts the video signals to YUV 16-bit digital video data (step 101), sends the converted video data to the video processor 21, and reduces the size of video data according to the display size (step 102). Video data from the video processor 21 is sent to one of two paths: real time output path 25 and capturing-only path 26.

Video data sent to the real time output path 25 is once stored in the off-screen memory 15 (step 103). The video data is then read from the off-screen memory 15 (step 104) and sent to the display control circuit 22 where the video data is processed in many ways. For example, enlargement, interpolation (conversion of interlace-compatible YUV 16-bit image data to non-interlace compatible image data), switching from video data to and from graphic data, and digital/analog signal conversion to produce analog RGB signals (step 105). Video data converted to analog RGB signals are output to the display 16 for display.

On the other hand, video data sent to the capturing-only path 26 is checked to see if the video data is to be captured (step 107). If the video data is not to be captured, the gate 23 is closed to stop data transfer (step 113). If the video data is to be captured, a FIFO memory control circuit in the gate 23 sends the enable signal to the FIFO memory 24 to store video data in the FIFO memory 24 (steps 108, 109).

Then, the system checks if the system bus 17 of the computer such as a PCI bus is being used by some other unit in the computer (step 110). If the PCI bus is not being used by any

other unit in the computer, the video data is sent from the FIFO memory 24 to the system memory 18 of the computer system via the PCI bus (step 111).

When the PCI bus is being used by some other unit in the computer system, the system checks to see if the video data in the FIFO memory 24 contains the field delimiter (step 112). If the video data contains the field delimiter, the system stops sending video data (step 113) at this point; if the video data does not contain the field delimiter, the system passes control back to step 108 to transfer the next video data to the FIFO memory 24.

Video data is sent to the FIFO memory 24 (step 109), stored there for a while, and then output (step 110). The FIFO memory 24, which has a constant input bandwidth of about 18Mbps and the maximum output bandwidth of 132Mbps, does not overflow during normal operation. In step 112, the presence of the frame delimiter, rather than the field delimiter, may be checked.

As described above, video data from the video processor is sent to the system bus not via the frame buffer. This means that video data may be captured into the system memory regardless of the status of the real time output path including the frame buffer. This increases the rate of capturing video data into the system memory.

On the other hand, the embodiment according to the present invention has two independent paths configured: one is

the real time output path via which video data is transferred to the display in real time and the other is the capturing-only path via which video data is transferred to the system memory. This configuration prevents the display of data on the display unit from being affected even when data is being captured. That is, the system keeps on sending video data to the display at a constant rate regardless of whether or not data is being captured, preventing data transfer to the display from being interrupted when data is being captured.

WHAT IS CLAIMED IS:

1. A video data transfer system comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer; and

a capturing-only path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus.

2. A video data transfer system as defined by claim 1, wherein

said real time output path comprises:

an off-screen memory which receives video data from said video processor via a data bus and stores video data therein, said off-screen memory being in the frame buffer; and

a display control circuit which receives video data read from said off-screen memory via said data bus for enlargement and interpolation processing and transfers processed results to said display, and wherein

said capturing-only circuit comprises:

a gate which is opened only when video data is received from said video processor for capturing; and

memory means for storing said video data sent through said gate and for transferring said video data to said system bus.

3. A video data transfer system as defined in claim 2, wherein

said memory means transfers said stored video data to said system bus when said system bus is not occupied by some

other unit and, when said system bus is occupied by some other unit, checks if said stored data contains a field delimiter or a frame delimiter and closes said gate to stop data transfer when said stored data contains the delimiter and, when said stored data does not contain the delimiter, stores the next video data passing through said gate.

ABSTRACT OF THE DISCLOSURE

A video data transfer system which increases the rate of capturing video data into a system memory without being affected by a data bus and which prevents the display of data on a display unit from being affected even when data is being captured. Video data from a video processor 21 is sent, not via a frame buffer 14 but via a capturing-only path 26, directly to a system bus 17. This means that video data may be captured into a system memory 18 regardless of the status of a real time output path 25. On the other hand, video data is sent to a display 16 via the real time output path 25 provided independently of the capturing-only path 26. This means that video data may be sent to the display 16 at a constant rate regardless of whether or not data is being captured.

FIG. 1

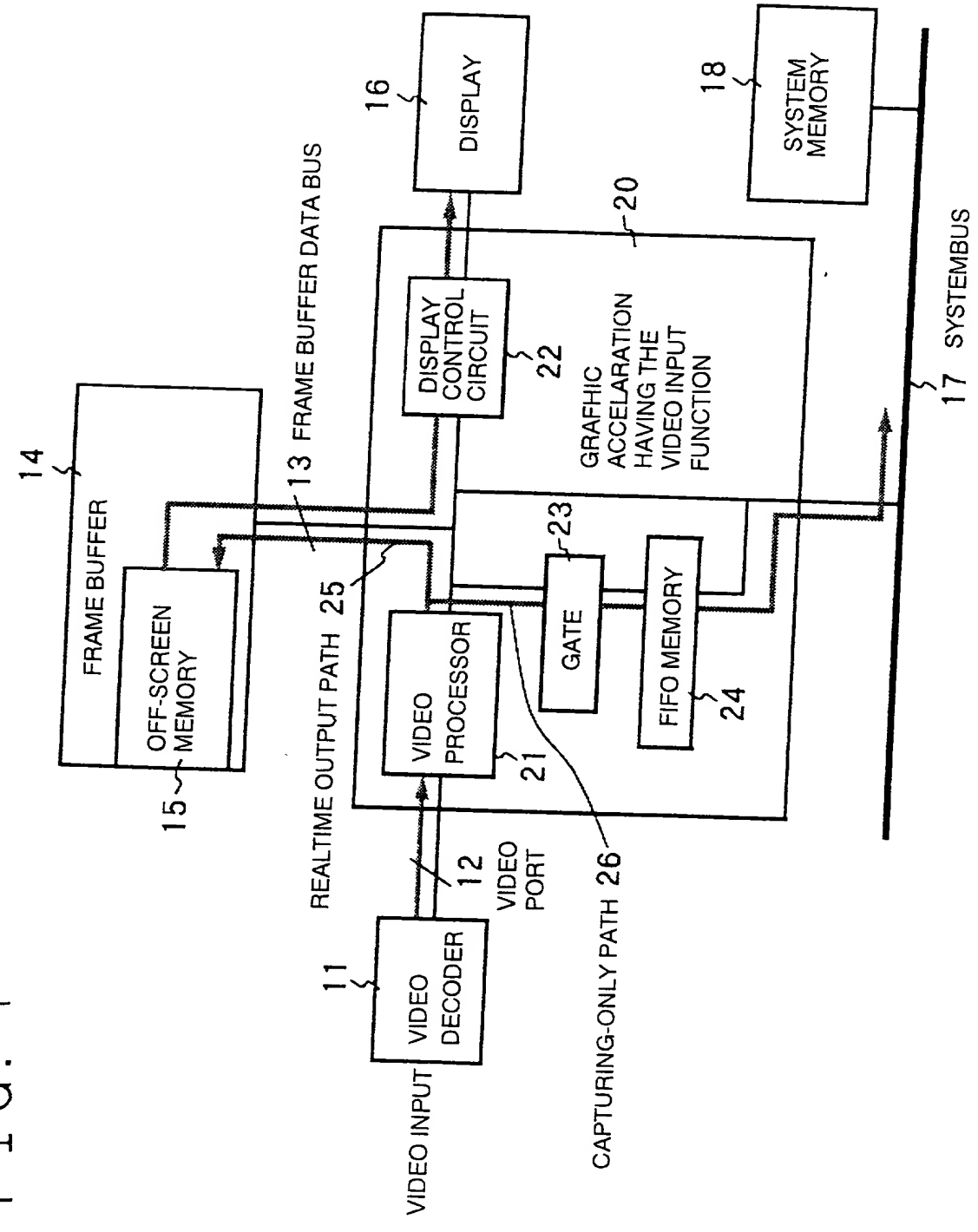

FRAME BUFFER
OFF-SCREEN MEMORY
15
14
13 FRAME BUFFER DATA BUS
16
DISPLAY
18
SYSTEM MEMORY
20
DISPLAY CONTROL CIRCUIT
22
GRAFHIC ACCELARATION HAVING THE VIDEO INPUT FUNCTION
17 SYSTEMBUS
23
GATE
FIFO MEMORY
24
REALTIME OUTPUT PATH 25
VIDEO PROCESSOR
21
VIDEO PORT
12
CAPTURING-ONLY PATH 26
11
VIDEO DECODER
VIDEO INPUT

FIG. 2

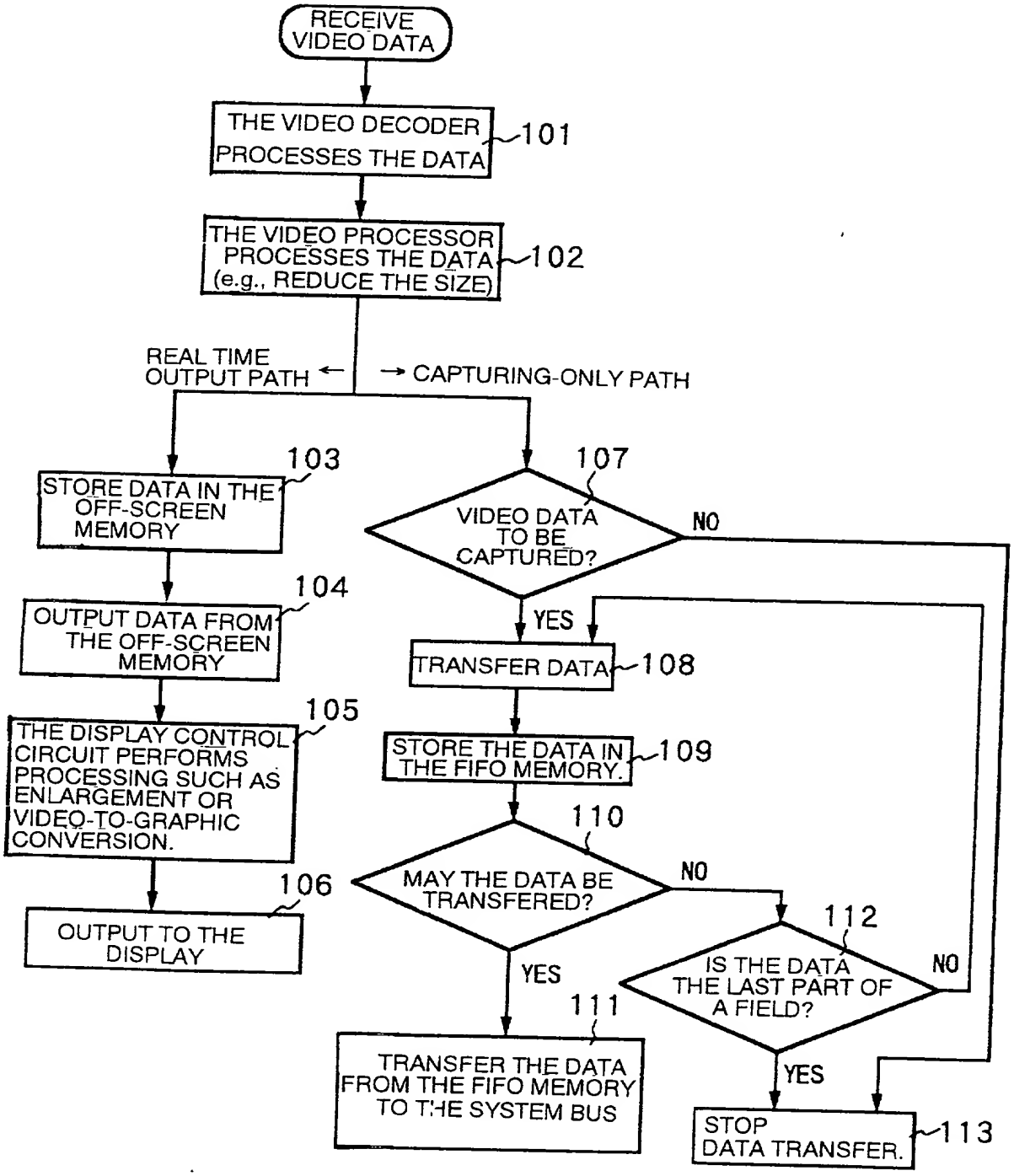
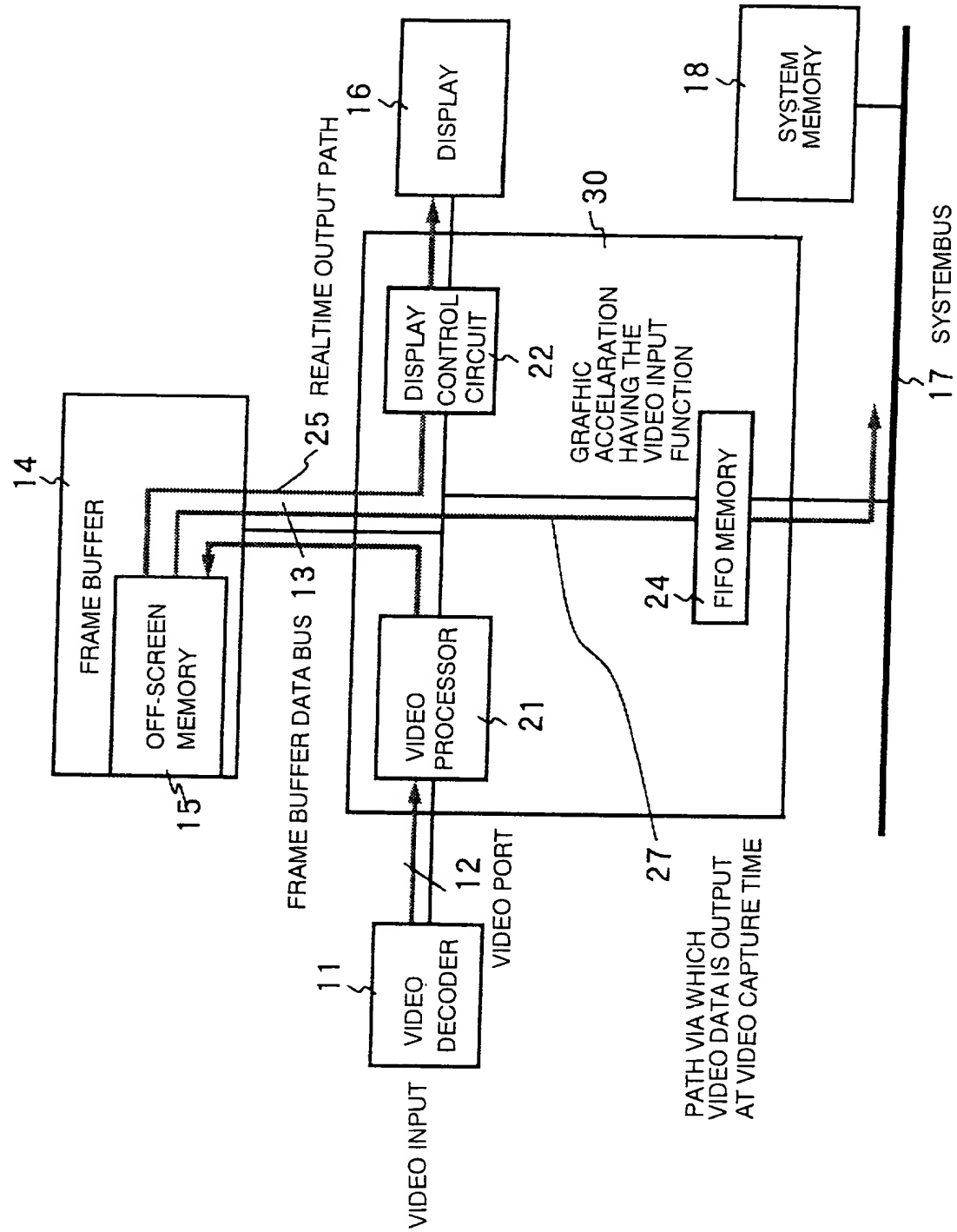

RECEIVE VIDEO DATA
THE VIDEO DECODER PROCESSES THE DATA
101
THE VIDEO PROCESSOR PROCESSES THE DATA (e.g., REDUCE THE SIZE)
102
REAL TIME OUTPUT PATH
CAPTURING-ONLY PATH
103
STORE DATA IN THE OFF-SCREEN MEMORY
104
OUTPUT DATA FROM THE OFF-SCREEN MEMORY
105
THE DISPLAY CONTROL CIRCUIT PERFORMS PROCESSING SUCH AS ENLARGEMENT OR VIDEO-TO-GRAPHIC CONVERSION.
106
OUTPUT TO THE DISPLAY
107
VIDEO DATA TO BE CAPTURED?
NO
YES
108
TRANSFER DATA
109
STORE THE DATA IN THE FIFO MEMORY.
110
MAY THE DATA BE TRANSFERED?
NO
YES
111
TRANSFER THE DATA FROM THE FIFO MEMORY TO THE SYSTEM BUS
112
IS THE DATA THE LAST PART OF A FIELD?
NO
YES
113
STOP DATA TRANSFER.

FIG. 3


14
FRAME BUFFER
OFF-SCREEN MEMORY
15
25 REALTIME OUTPUT PATH
16
DISPLAY
18
SYSTEM MEMORY
30
DISPLAY CONTROL CIRCUIT
22
GRAFHIC ACCELARATION HAVING THE VIDEO INPUT FUNCTION
FRAME BUFFER DATA BUS 13
VIDEO PROCESSOR
21
FIFO MEMORY
24
17 SYSTEMBUS
27
PATH VIA WHICH VIDEO DATA IS OUTPUT AT VIDEO CAPTURE TIME
11
VIDEO DECODER
12
VIDEO PORT
VIDEO INPUT

UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION	OFGS FILE NO. P/3156-3

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Video Data Transfer System

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	112117/1997	30/4/1997	YES X NO ____
			YES ____ NO ____
			YES ____ NO ____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	STATUS (patented, pending, abandoned)

I hereby appoint OSTROLENK, FABER, GERB & SOFFEN, and the members of the firm, Marvin C. Soffen - Reg. No. 17,542; Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944 and Louis C. Dujmich - Reg. No. 30,625, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE	DATE
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RESIDENCE	COUNTRY OF CITIZENSHIP

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RESIDENCE	COUNTRY OF CITIZENSHIP

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